PA04 • PA04A

FEATURES

- HIGH INTERNAL DISSIPATION — 200 WATTS
- HIGH VOLTAGE, HIGH CURRENT — 200V, 20A
- HIGH SLEW RATE — 50V/µS
- 4 WIRE CURRENT LIMIT SENSING
- LOW DISTORTION
- EXTERNAL SLEEP MODE CONTROL
- OPTIONAL BOOST VOLTAGE INPUTS
- EVALUATION KIT — SEE EK09

APPLICATIONS

- SONAR TRANSDUCER DRIVER
- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ±95V
- AUDIO UP TO 400W

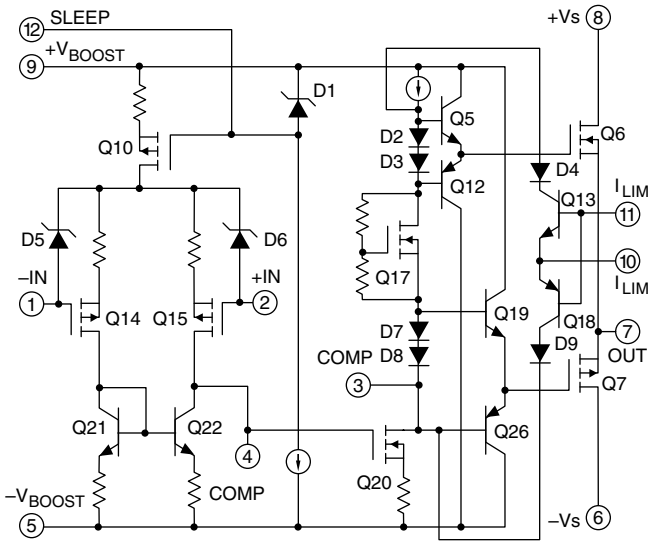
DESCRIPTION

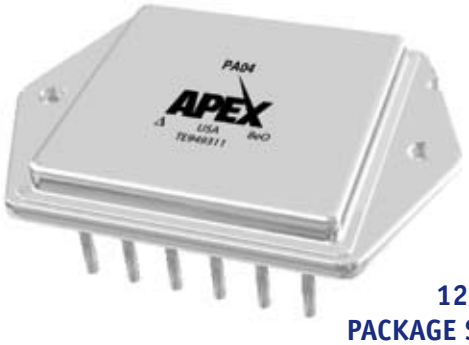
The PA04 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

The PA04 is a highly flexible amplifier. The sleep mode feature allows ultra-low quiescent current for standby operation or load protection by disabling the entire amplifier. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors performance to user needs. A four wire sense technique allows precision current limiting without the need to consider internal or external milliohm parasitic resistance in the output line.

The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers will void product warranty.

EQUIVALENT SCHEMATIC

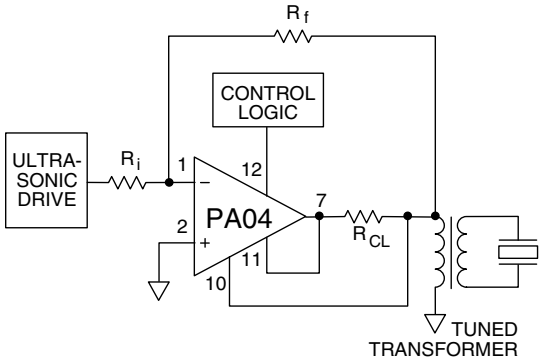




12-PIN DIP
PACKAGE STYLE CR

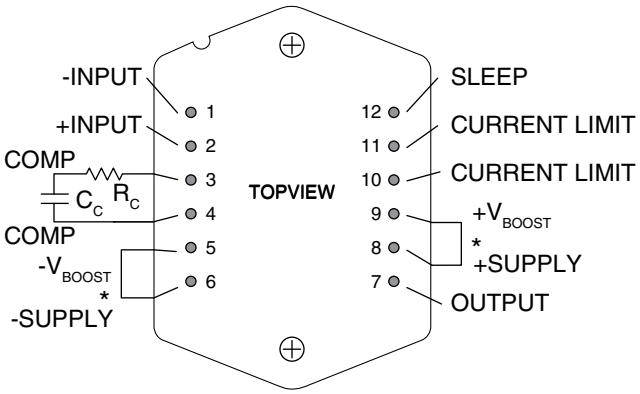
TYPICAL APPLICATION

The high power bandwidth and high voltage output of the PA04 allows driving sonar transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the PA04. Control logic turns off the amplifier in sleep mode.



Sonar Transducer Driver

EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_C	R_C
1	470pF	120Ω
>3	220pF	120Ω
≥10	100pF	120Ω

C_C RATED FOR FULL SUPPLY VOLTAGE
*See "BOOST OPERATION" paragraph.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
BOOST VOLTAGE	SUPPLY VOLTAGE +20V
OUTPUT CURRENT, within SOA	20A
POWER DISSIPATION, internal	200W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA04 MIN	PA04 TYP	PA04 MAX	PA04A MIN	PA04A TYP	PA04A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			5	10		2	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		30	50		10	30	µV/°C
OFFSET VOLTAGE, vs. supply			15			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		30			10		µV/W
BIAS CURRENT, initial			10	50		5	20	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		5	20	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			13			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_B$-8			*			V
COMMON MODE REJECTION, DC	Full temp. range, V_{CM} = ±20V	86	98		*	*		dB
INPUT NOISE	100kHz BW, R_S = 1KΩ		10			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	Full temperature range, C_C = 100pF	94	102		*	*		dB
GAIN BANDWIDTH PRODUCT	I_O = 10A		2			*		MHz
POWER BANDWIDTH	R_L = 4.5Ω, V_O = 180V p-p C_C = 100pF, R_C = 120Ω		90			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING	I_O = 15A	$\pm V_S$-8.8	$\pm V_S$-7.5		*	*		V
VOLTAGE SWING	V_{BOOST} = Vs + 5V, I_O = 20A	$\pm V_S$-6.8	$\pm V_S$-5.5		*	*		V
CURRENT, peak		20			*			A
SETTLING TIME to .1%	A_V = 1, 10V step, R_L = 4Ω		2.5			*		µs
SLEW RATE	A_V = 10, C_C = 100pF, R_C = 120Ω	40	50			*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = +1	10			*			nF
RESISTANCE			2			*		Ω
POWER SUPPLY								
VOLTAGE	Full temperature range	±15	±75	±100	*	*	*	V
CURRENT, quiescent, boost supply			30	40		*	*	mA
CURRENT, quiescent, total			70	90		*	*	mA
CURRENT, quiescent, total, sleep mode	Full temperature range		3	5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz		.3	.4		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz		.5	.6		*	*	°C/W
RESISTANCE[4], junction to air	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		85	*		*	°C

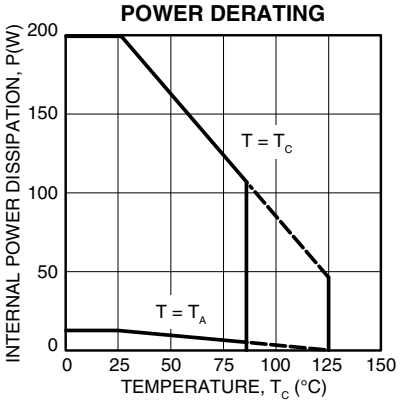
NOTES: * The specification of PA04A is identical to the specification for PA04 in applicable column to the left.
1. Unless otherwise noted: T_C = 25°C, C_C = 470pF, R_C = 120 ohms. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_{BOOST} = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The PA04 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.

CAUTION

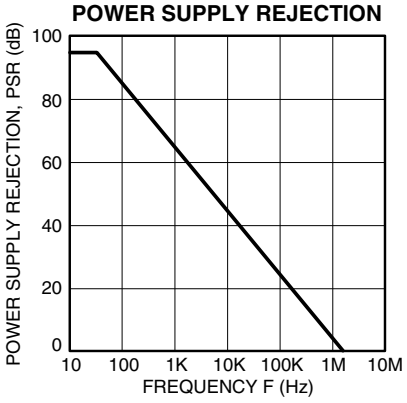
The PA04 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

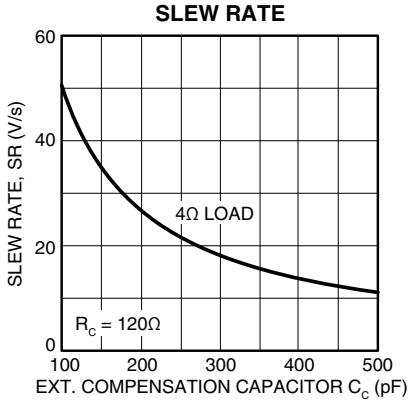
POWER DERATING



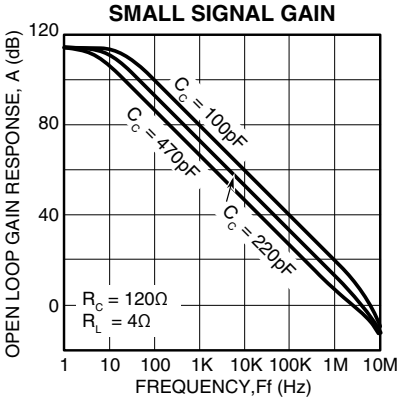
POWER SUPPLY REJECTION



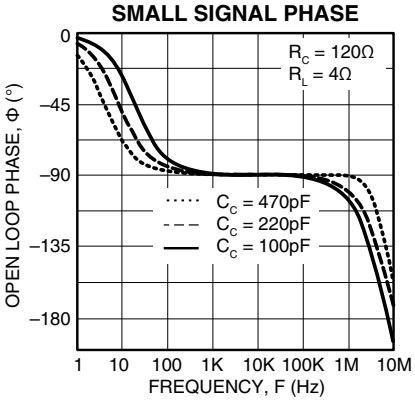
SLEW RATE



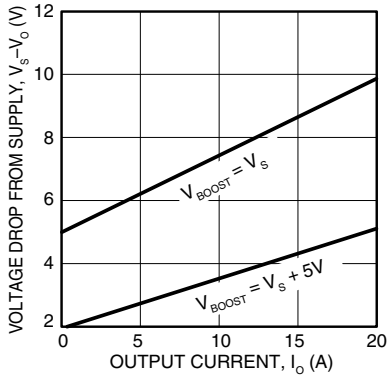
SMALL SIGNAL GAIN



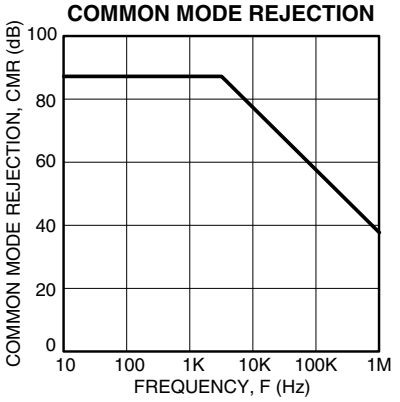
SMALL SIGNAL PHASE



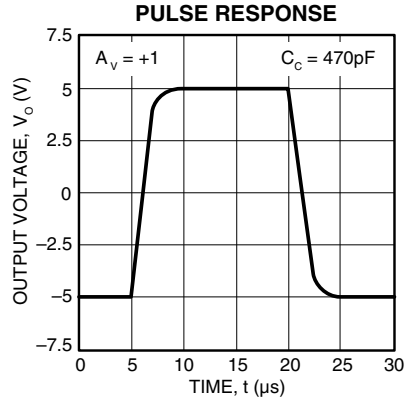
OUTPUT VOLTAGE SWING



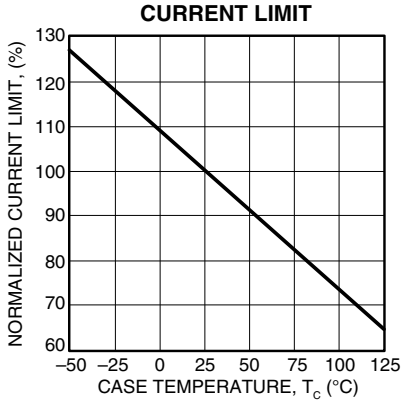
COMMON MODE REJECTION



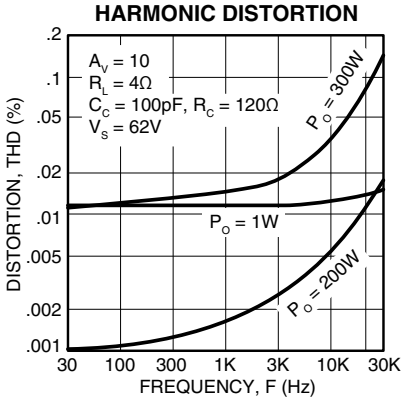
PULSE RESPONSE



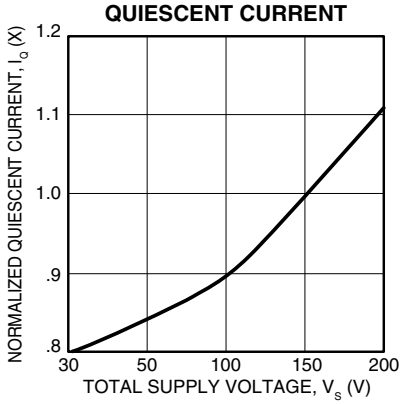
CURRENT LIMIT



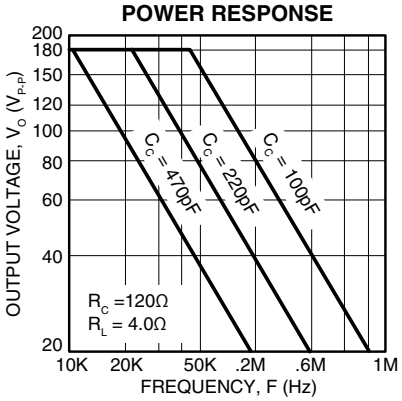
HARMONIC DISTORTION



QUIESCENT CURRENT



POWER RESPONSE



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

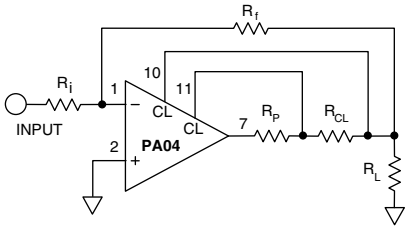
CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 11 must be connected to the amplifier output side and pin 10 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1. This connection will bypass any parasitic resistances, Rp, formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1.

The value of the current limit resistor can be calculated as follows:

$$R_{CL} = \frac{.76}{I_{LIMIT}}$$

Figure 1.
Current Limit.

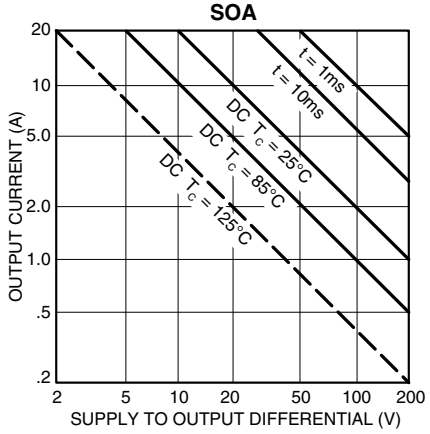


SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



SLEEP MODE OPERATION

In the sleep mode, pin 12 (sleep) is tied to pin 9 ($+V_{BOOST}$). This disables the amplifier's internal reference and the amplifier shuts down except for a trickle current of 3 mA which flows into pin 12. Pin 12 should be left open if the sleep mode is not required.

Several possible circuits can be built to take advantage of this mode. In Figure 2A a small signal relay is driven by a logic gate. This removes the requirement to deal with the common mode voltage that exists on the shutoff circuitry since the sleep mode is referenced to the $+V_{BOOST}$ voltage.

In Figure 2B, circuitry is used to level translate the sleep mode input signal. The differential input activates sleep mode with a differential logic level signal and allows common mode voltages to $\pm V_{BOOST}$.

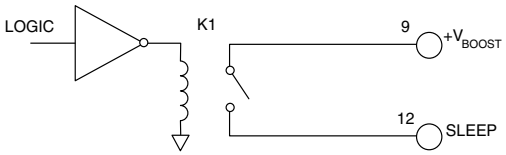


FIGURE 2A. SLEEP MODE CIRCUIT.

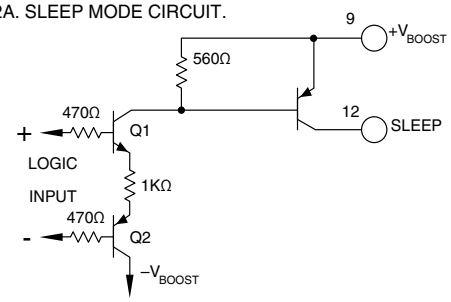


FIGURE 2B. SLEEP MODE CIRCUIT.

BOOST OPERATION

With the V_{BOOST} feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 9) and $-V_{BOOST}$ (pin 5) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 8) and $-V_S$ (pin 6) are connected to the high current output stage. An additional 5V on the V_{BOOST} pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $-V_{BOOST}$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 3 and 4. Unity gain stability can be achieved at any compensation capacitance greater than 330 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C and R_C for the application.